

FIG. 1

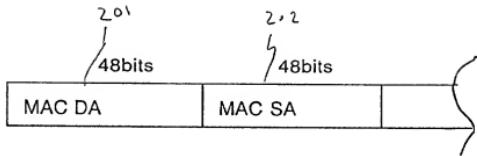


FIG. 2

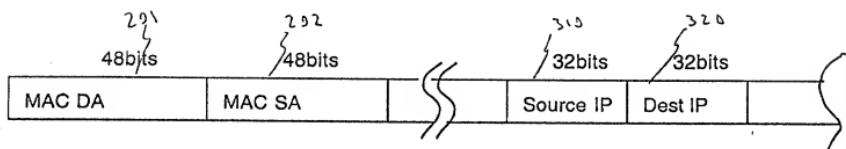


FIG. 3

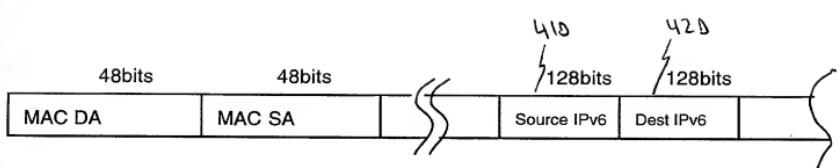


FIG. 4

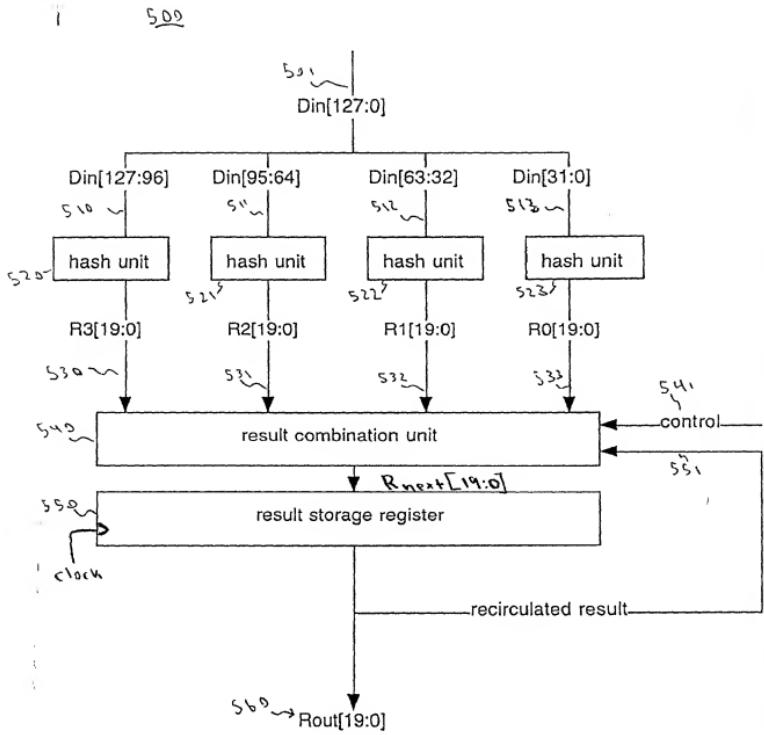


FIG. 5

```
if (control == 0)
{
    Rnext = R3 XOR R2 XOR R1 XOR R0;
}
else
{
    Rnext = R3 XOR R2 XOR R1 XOR R0 XOR Rout;
}
```

$R_{out} \leftarrow R_{next}$ on each positive clock edge

FIG. 6

700

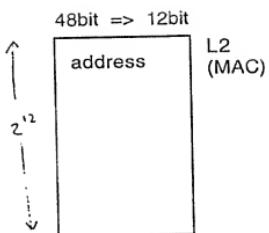


FIG. 7

805

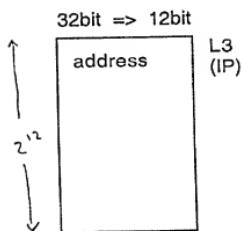


FIG. 8

905

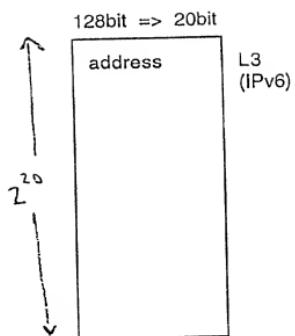


FIG. 9

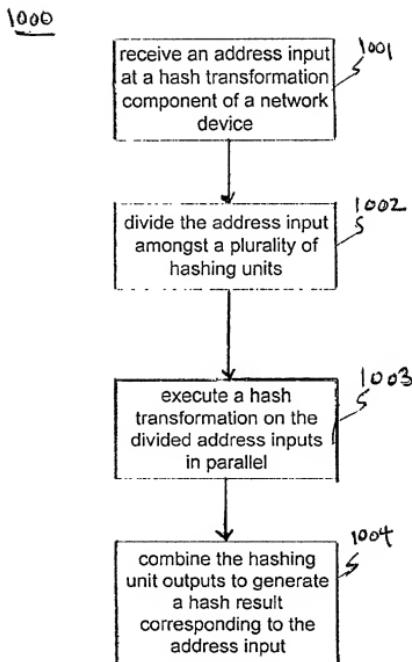


FIG. 10